

74LV4051

8-channel analog multiplexer/demultiplexer

Rev. 8 — 16 July 2021

Product data sheet

1. General description

The 74LV4051 is an 8-channel analog multiplexer/demultiplexer with three digital select inputs (S0 to S2), an active-LOW enable input (\bar{E}), eight independent inputs/outputs (Y0 to Y7) and a common input/output (Z). It is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC4051 and 74HCT4051. With \bar{E} LOW, one of the eight switches is selected (low impedance ON-state) by S0 to S2. With \bar{E} HIGH, all switches are in the high-impedance OFF-state, independent of S0 to S2.

V_{CC} and GND are the supply voltage pins for the digital control inputs (S0 to S2, and \bar{E}). The V_{CC} to GND ranges are 1.0 V to 6.0 V. The analog inputs/outputs (Y0 to Y7, and Z) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 6.0 V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

2. Features and benefits

- Optimized for low-voltage applications: 1.0 V to 6.0 V
- Accepts TTL input levels between $V_{CC} = 2.7$ V and $V_{CC} = 3.6$ V
- Low ON resistance:
 - 145 Ω (typical) at $V_{CC} - V_{EE} = 2.0$ V
 - 80 Ω (typical) at $V_{CC} - V_{EE} = 3.0$ V
 - 60 Ω (typical) at $V_{CC} - V_{EE} = 4.5$ V
- Logic level translation:
 - To enable 3 V logic to communicate with ± 3 V analog signals
- Typical 'break before make' built in
- ESD protection:
 - HBM JESD22-A114E exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|-------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | |
| 74LV4051D | -40 °C to +125 °C | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| 74LV4051PW | -40 °C to +125 °C | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |
| 74LV4051BQ | -40 °C to +125 °C | DHVQFN16 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm | SOT763-1 |

4. Functional diagram

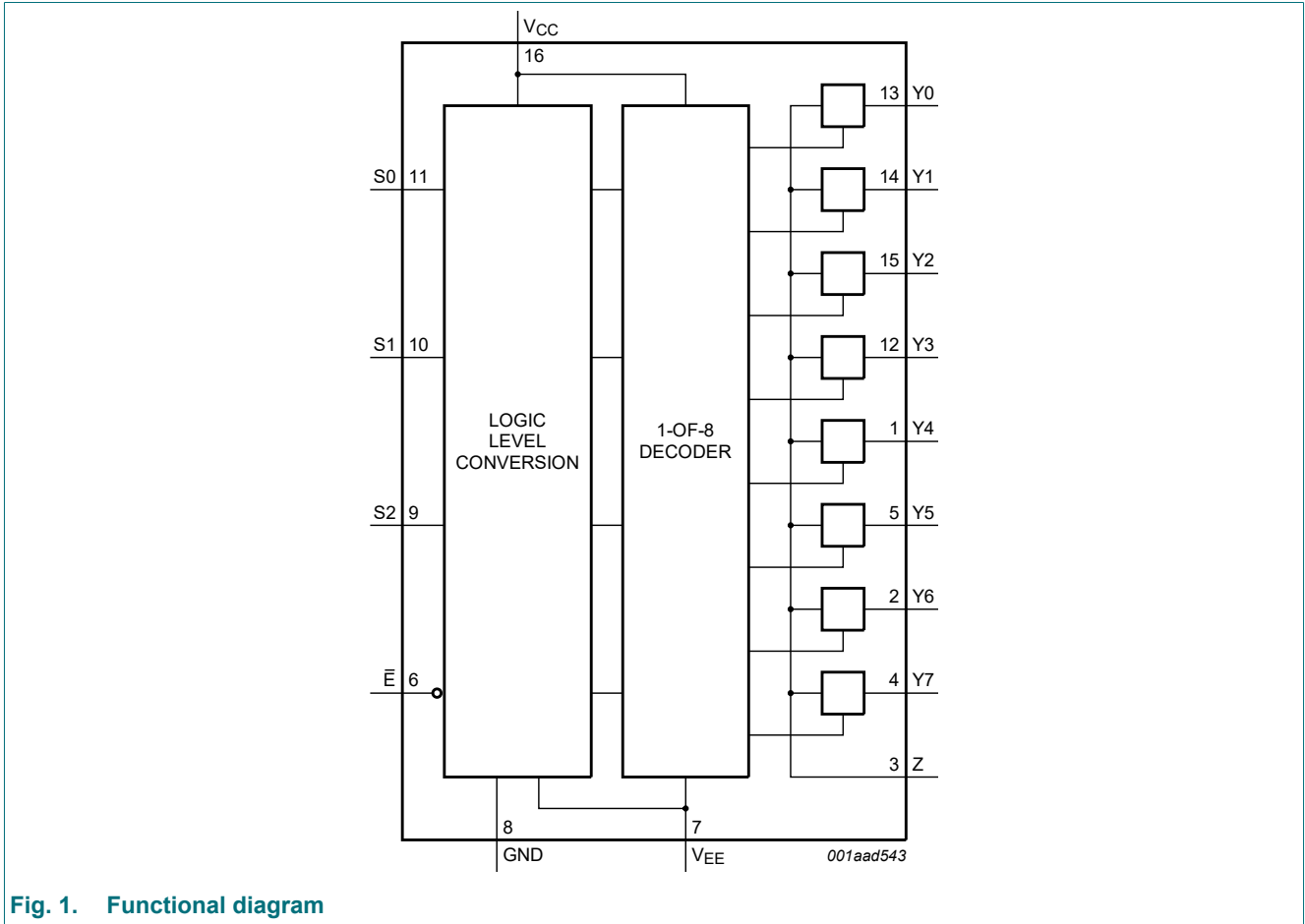


Fig. 1. Functional diagram

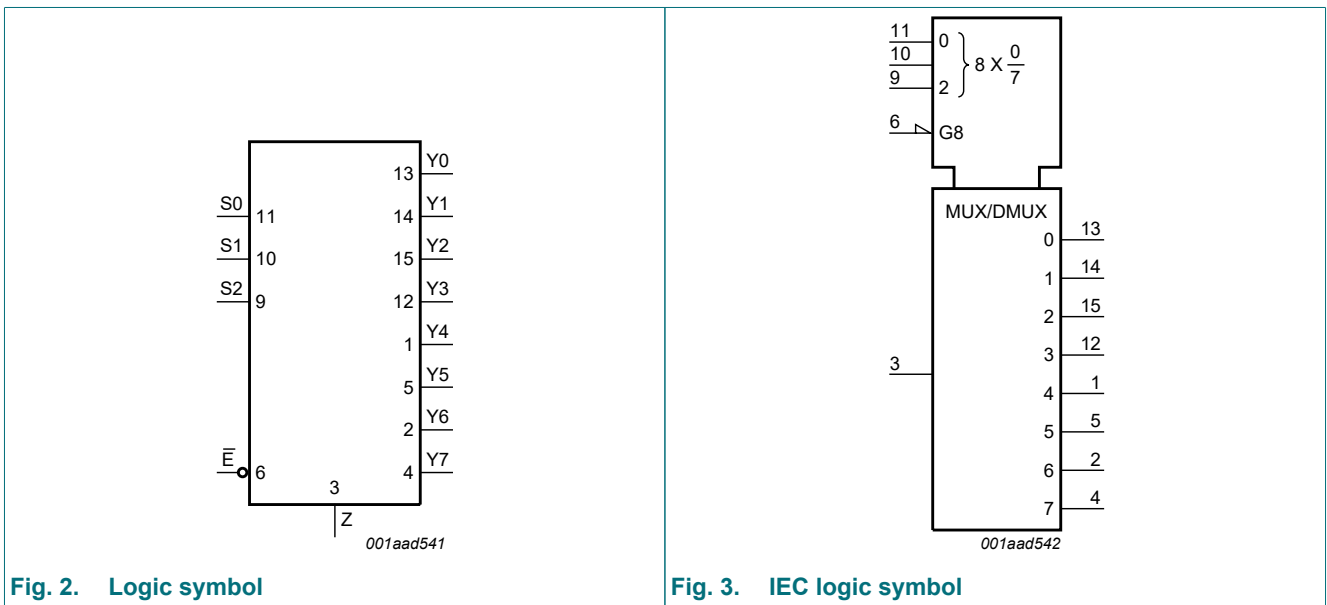


Fig. 2. Logic symbol

Fig. 3. IEC logic symbol

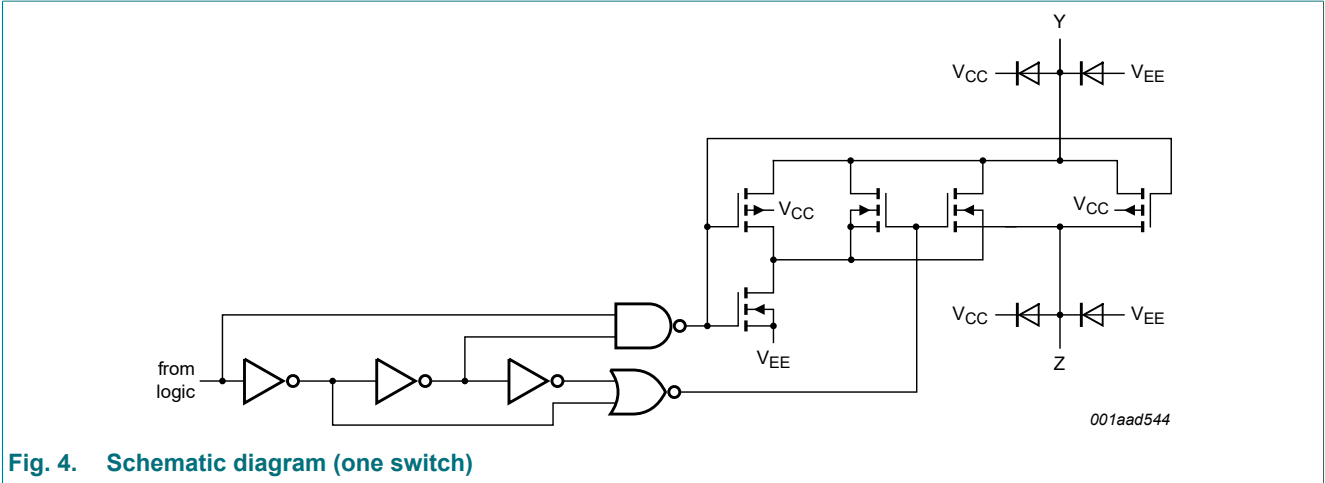


Fig. 4. Schematic diagram (one switch)

5. Pinning information

5.1. Pinning

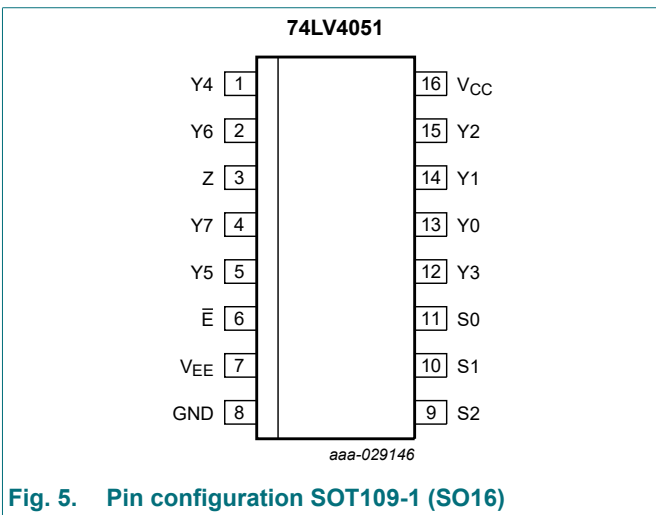


Fig. 5. Pin configuration SOT109-1 (SO16)

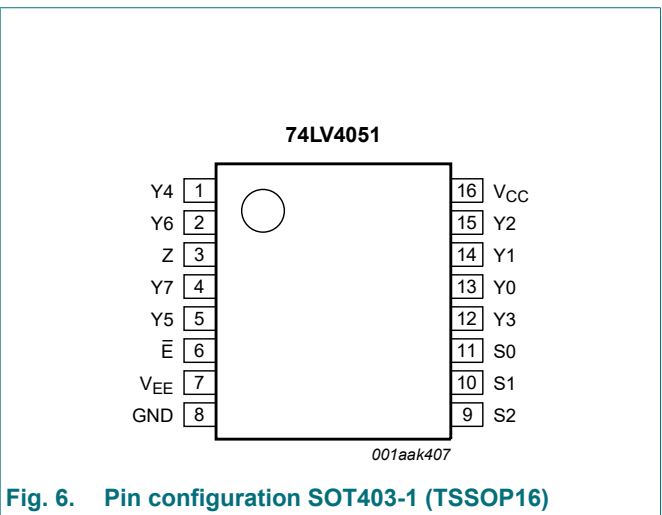


Fig. 6. Pin configuration SOT403-1 (TSSOP16)

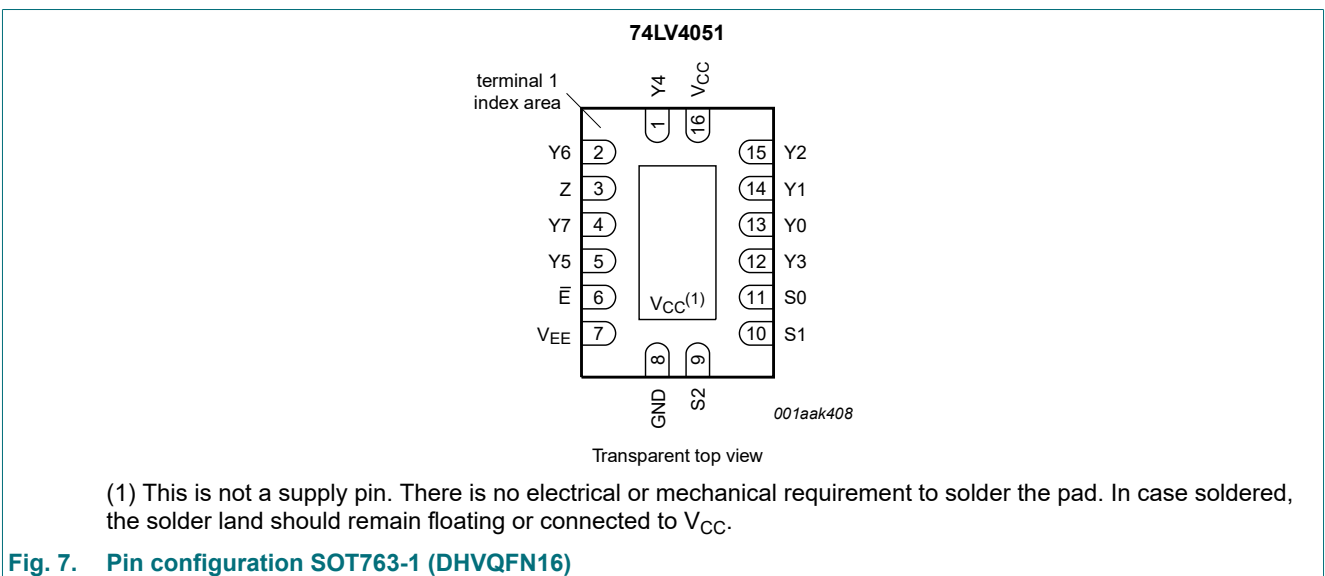


Fig. 7. Pin configuration SOT763-1 (DHVQFN16)

5.2. Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|--------------------------------|----------------------------|-----------------------------|
| \bar{E} | 6 | enable input (active LOW) |
| V_{EE} | 7 | supply voltage |
| GND | 8 | ground supply voltage |
| S0, S1, S2 | 11, 10, 9 | select input |
| Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7 | 13, 14, 15, 12, 1, 5, 2, 4 | independent input or output |
| Z | 3 | common output or input |
| V_{CC} | 16 | supply voltage |

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

| Input | | | | Channel ON |
|-----------|----|----|----|--------------|
| \bar{E} | S2 | S1 | S0 | |
| L | L | L | L | Y0 to Z |
| L | L | L | H | Y1 to Z |
| L | L | H | L | Y2 to Z |
| L | L | H | H | Y3 to Z |
| L | H | L | L | Y4 to Z |
| L | H | L | H | Y5 to Z |
| L | H | H | L | Y6 to Z |
| L | H | H | H | Y7 to Z |
| H | X | X | X | switches off |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND = 0 V.

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|---|------|----------|------|
| V_{CC} | supply voltage | [1] | -0.5 | +7.0 | V |
| I_{IK} | input clamping current | $V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$ [2] | - | ± 20 | mA |
| I_{SK} | switch clamping current | $V_{SW} < -0.5 \text{ V}$ or $V_{SW} > V_{CC} + 0.5 \text{ V}$ [2] | - | ± 20 | mA |
| I_{SW} | switch current | $V_{SW} > -0.5 \text{ V}$ or $V_{SW} < V_{CC} + 0.5 \text{ V}$; source or sink current [2] | - | ± 25 | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40 \text{ °C}$ to $+125 \text{ °C}$ [3] | - | 500 | mW |

- [1] To avoid drawing V_{CC} current out of terminal Z, when switch current flows into terminals Yn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{CC} current will flow out of terminals Yn, and in this case there is no limit for the voltage drop across the switch, but the voltages at Yn and Z may not exceed V_{CC} or V_{EE} .
- [2] The minimum input voltage rating may be exceeded if the input current rating is observed.
- [3] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|---|-----|-----|----------|------|
| V_{CC} | supply voltage | see Fig. 8 [1] | 1 | 3.3 | 6 | V |
| V_I | input voltage | | 0 | - | V_{CC} | V |
| V_{SW} | switch voltage | | 0 | - | V_{CC} | V |
| T_{amb} | ambient temperature | in free air | -40 | - | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 1.0\text{ V to }2.0\text{ V}$ | - | - | 500 | ns/V |
| | | $V_{CC} = 2.0\text{ V to }2.7\text{ V}$ | - | - | 200 | ns/V |
| | | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | - | - | 100 | ns/V |

[1] The static characteristics are guaranteed from $V_{CC} = 1.2\text{ V}$ to 6.0 V , but LV devices are guaranteed to function down to $V_{CC} = 1.0\text{ V}$ (with input levels GND or V_{CC}).

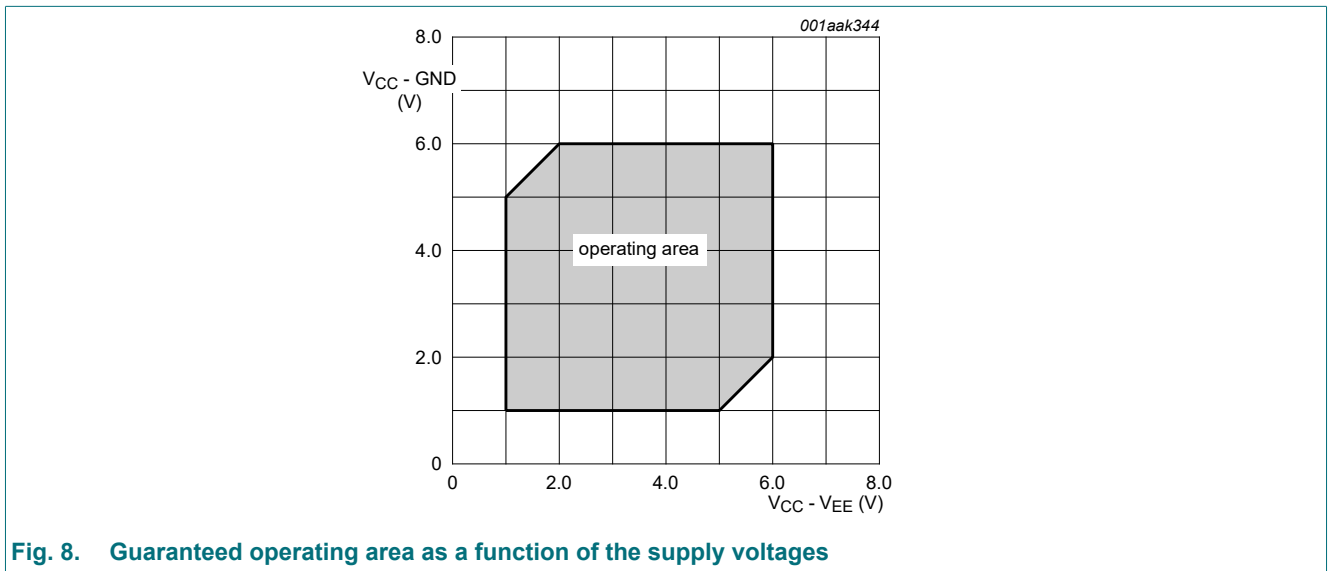


Fig. 8. Guaranteed operating area as a function of the supply voltages

9. Static characteristics

Table 6. Static characteristics

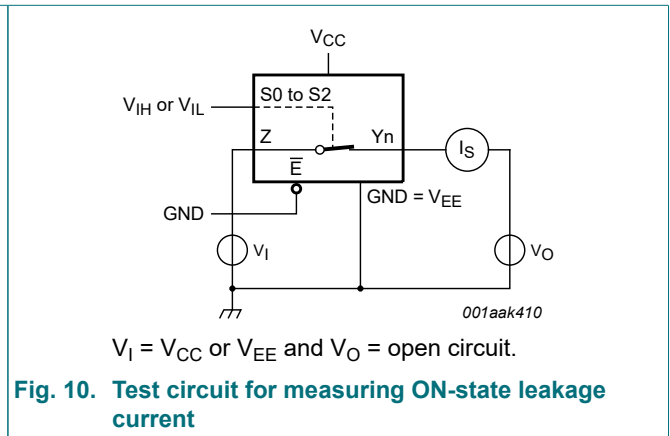
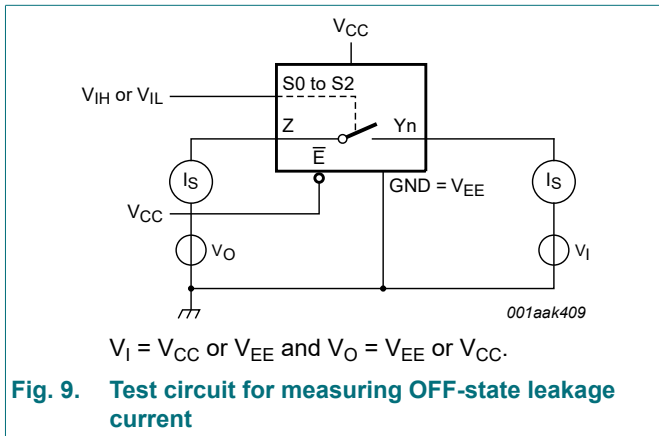
At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|----------|--------------------------|---|------------------|--------|------|-------------------|------|------|
| | | | Min | Typ[1] | Max | Min | Max | |
| V_{IH} | HIGH-level input voltage | $V_{CC} = 1.2\text{ V}$ | 0.9 | - | - | 0.9 | - | V |
| | | $V_{CC} = 2.0\text{ V}$ | 1.4 | - | - | 1.4 | - | V |
| | | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | 2.0 | - | - | 2.0 | - | V |
| | | $V_{CC} = 4.5\text{ V}$ | 3.15 | - | - | 3.15 | - | V |
| | | $V_{CC} = 6.0\text{ V}$ | 4.20 | - | - | 4.20 | - | V |
| V_{IL} | LOW-level input voltage | $V_{CC} = 1.2\text{ V}$ | - | - | 0.3 | - | 0.3 | V |
| | | $V_{CC} = 2.0\text{ V}$ | - | - | 0.6 | - | 0.6 | V |
| | | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | - | - | 0.8 | - | 0.8 | V |
| | | $V_{CC} = 4.5\text{ V}$ | - | - | 1.35 | - | 1.35 | V |
| | | $V_{CC} = 6.0\text{ V}$ | - | - | 1.80 | - | 1.80 | V |

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|---------------------|---------------------------|---|------------------|--------|-----|-------------------|-----|------|
| | | | Min | Typ[1] | Max | Min | Max | |
| I _I | input leakage current | V _I = V _{CC} or GND | | | | | | |
| | | V _{CC} = 3.6 V | - | - | 1.0 | - | 1.0 | μA |
| | | V _{CC} = 6.0 V | - | - | 2.0 | - | 2.0 | μA |
| I _{S(OFF)} | OFF-state leakage current | V _I = V _{IH} or V _{IL} ; see Fig. 9 | | | | | | |
| | | V _{CC} = 3.6 V | - | - | 1.0 | - | 1.0 | μA |
| | | V _{CC} = 6.0 V | - | - | 2.0 | - | 2.0 | μA |
| I _{S(ON)} | ON-state leakage current | V _I = V _{IH} or V _{IL} ; see Fig. 10 | | | | | | |
| | | V _{CC} = 3.6 V | - | - | 1.0 | - | 1.0 | μA |
| | | V _{CC} = 6.0 V | - | - | 2.0 | - | 2.0 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A | | | | | | |
| | | V _{CC} = 3.6 V | - | - | 20 | - | 40 | μA |
| | | V _{CC} = 6.0 V | - | - | 40 | - | 80 | μA |
| ΔI _{CC} | additional supply current | per input; V _I = V _{CC} - 0.6 V; V _{CC} = 2.7 V to 3.6 V | - | - | 500 | - | 850 | μA |
| C _I | input capacitance | | - | 3.5 | - | - | - | pF |
| C _{sw} | switch capacitance | independent pins Y _n | - | 5 | - | - | - | pF |
| | | common pin Z | - | 25 | - | - | - | pF |

[1] Typical values are measured at T_{amb} = 25 °C.

9.1. Test circuits



9.2. ON resistance

Table 7. ON resistance

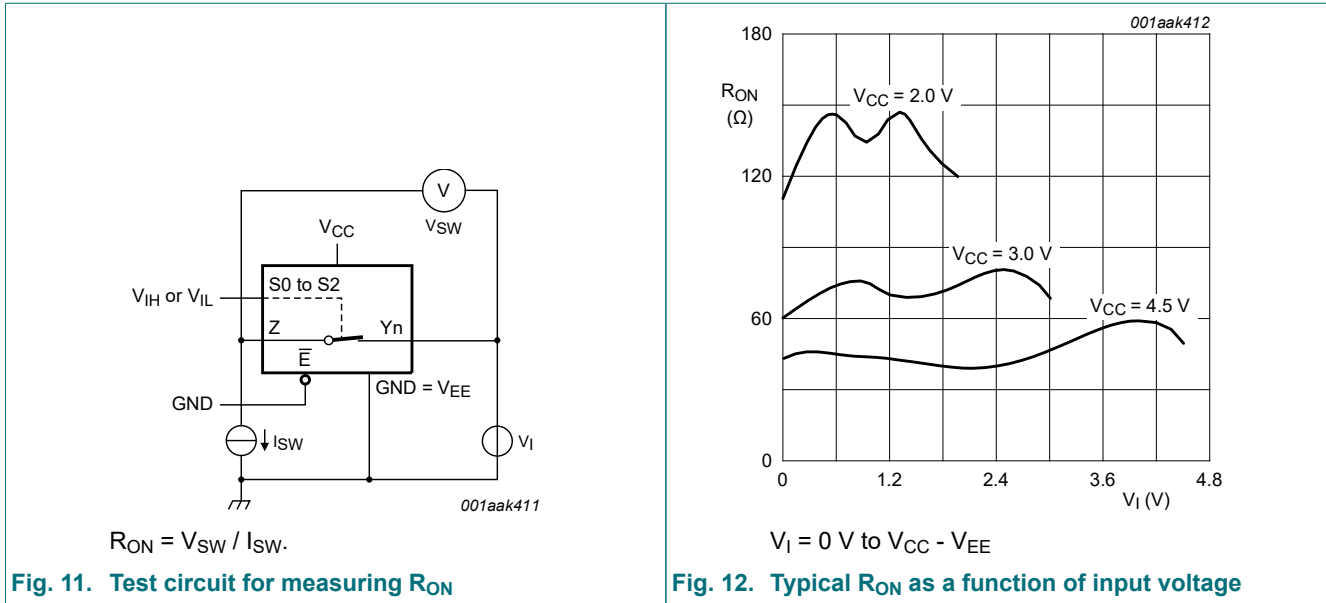
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit and graph see [Fig. 11](#) and [Fig. 12](#).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|-----------------------|---|--|------------------|---------|-----|-------------------|-----|------|
| | | | Min | Typ [1] | Max | Min | Max | |
| R _{ON(peak)} | ON resistance (peak) | V _I = 0 V to V _{CC} - V _{EE} | | | | | | |
| | | V _{CC} = 1.2 V; I _{SW} = 100 μA [2] | - | - | - | - | - | Ω |
| | | V _{CC} = 2.0 V; I _{SW} = 1000 μA | - | 145 | 325 | - | 375 | Ω |
| | | V _{CC} = 2.7 V; I _{SW} = 1000 μA | - | 90 | 200 | - | 235 | Ω |
| | | V _{CC} = 3.0 V to 3.6 V; I _{SW} = 1000 μA | - | 80 | 180 | - | 210 | Ω |
| | | V _{CC} = 4.5 V; I _{SW} = 1000 μA | - | 60 | 135 | - | 160 | Ω |
| | | V _{CC} = 6.0 V; I _{SW} = 1000 μA | - | 55 | 125 | - | 145 | Ω |
| ΔR _{ON} | ON resistance mismatch between channels | V _I = 0 V to V _{CC} - V _{EE} | | | | | | |
| | | V _{CC} = 1.2 V; I _{SW} = 100 μA [2] | - | - | - | - | - | Ω |
| | | V _{CC} = 2.0 V; I _{SW} = 1000 μA | - | 5 | - | - | - | Ω |
| | | V _{CC} = 2.7 V; I _{SW} = 1000 μA | - | 4 | - | - | - | Ω |
| | | V _{CC} = 3.0 V to 3.6 V; I _{SW} = 1000 μA | - | 4 | - | - | - | Ω |
| | | V _{CC} = 4.5 V; I _{SW} = 1000 μA | - | 3 | - | - | - | Ω |
| | | V _{CC} = 6.0 V; I _{SW} = 1000 μA | - | 2 | - | - | - | Ω |
| R _{ON(rail)} | ON resistance (rail) | V _I = GND | | | | | | |
| | | V _{CC} = 1.2 V; I _{SW} = 100 μA [2] | - | 225 | - | - | - | Ω |
| | | V _{CC} = 2.0 V; I _{SW} = 1000 μA | - | 110 | 235 | - | 270 | Ω |
| | | V _{CC} = 2.7 V; I _{SW} = 1000 μA | - | 70 | 145 | - | 165 | Ω |
| | | V _{CC} = 3.0 V to 3.6 V; I _{SW} = 1000 μA | - | 60 | 130 | - | 150 | Ω |
| | | V _{CC} = 4.5 V; I _{SW} = 1000 μA | - | 45 | 100 | - | 115 | Ω |
| | | V _{CC} = 6.0 V; I _{SW} = 1000 μA | - | 40 | 85 | - | 100 | Ω |
| R _{ON(rail)} | ON resistance (rail) | V _I = V _{CC} - V _{EE} | | | | | | |
| | | V _{CC} = 1.2 V; I _{SW} = 100 μA [2] | - | 250 | - | - | - | Ω |
| | | V _{CC} = 2.0 V; I _{SW} = 1000 μA | - | 120 | 320 | - | 370 | Ω |
| | | V _{CC} = 2.7 V; I _{SW} = 1000 μA | - | 75 | 195 | - | 225 | Ω |
| | | V _{CC} = 3.0 V to 3.6 V; I _{SW} = 1000 μA | - | 70 | 175 | - | 205 | Ω |
| | | V _{CC} = 4.5 V; I _{SW} = 1000 μA | - | 50 | 130 | - | 150 | Ω |
| | | V _{CC} = 6.0 V; I _{SW} = 1000 μA | - | 45 | 120 | - | 135 | Ω |

[1] All typical values are measured at nominal V_{CC} and at T_{amb} = 25 °C.

[2] When supply voltages (V_{CC} - V_{EE}) near 1.2 V the analog switch ON resistance becomes extremely non-linear. When using a supply of 1.2 V, it is recommended to use these devices only for transmitting digital signals.

9.3. On resistance test circuit and graph



10. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (GND = $V_{EE} = 0$ V). For test circuit see [Fig. 15](#).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|----------|-------------------|--|------------------|---------|-----|-------------------|-----|------|
| | | | Min | Typ [1] | Max | Min | Max | |
| t_{pd} | propagation delay | Y_n to Z, Z to Y_n ; see Fig. 13 [2] | - | | | | | |
| | | $V_{CC} = 1.2$ V | - | 25 | - | - | - | ns |
| | | $V_{CC} = 2.0$ V | - | 9 | 17 | - | 20 | ns |
| | | $V_{CC} = 2.7$ V | - | 6 | 13 | - | 15 | ns |
| | | $V_{CC} = 3.0$ V to 3.6 V | - | 5 | 10 | - | 12 | ns |
| | | $V_{CC} = 4.5$ V | - | 4 | 9 | - | 10 | ns |
| | | $V_{CC} = 6.0$ V | - | 3 | 8 | - | 8 | ns |

8-channel analog multiplexer/demultiplexer

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|------------------|-------------------------------|---|------------------|---------|-----|-------------------|-----|------|
| | | | Min | Typ [1] | Max | Min | Max | |
| t _{en} | enable time | \bar{E} to Yn, Z; see Fig. 14 [2] | | | | | | |
| | | V _{CC} = 1.2 V | - | 145 | - | - | - | ns |
| | | V _{CC} = 2.0 V | - | 49 | 94 | - | 112 | ns |
| | | V _{CC} = 2.7 V | - | 36 | 69 | - | 83 | ns |
| | | V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF | - | 23 | - | - | - | ns |
| | | V _{CC} = 3.0 V to 3.6 V | - | 28 | 55 | - | 66 | ns |
| | | V _{CC} = 4.5 V | - | 25 | 47 | - | 56 | ns |
| | | V _{CC} = 6.0 V | - | 19 | 38 | - | 43 | ns |
| | | Sn to Yn; see Fig. 14 [2] | | | | | | |
| | | V _{CC} = 1.2 V | - | 140 | - | - | - | ns |
| | | V _{CC} = 2.0 V | - | 48 | 90 | - | 107 | ns |
| | | V _{CC} = 2.7 V | - | 35 | 66 | - | 79 | ns |
| | | V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF | - | 22 | - | - | - | ns |
| | | V _{CC} = 3.0 V to 3.6 V | - | 27 | 53 | - | 63 | ns |
| | | V _{CC} = 4.5 V | - | 24 | 45 | - | 54 | ns |
| | | V _{CC} = 6.0 V | - | 18 | 34 | - | 41 | ns |
| t _{dis} | disable time | \bar{E} to Yn, Z; see Fig. 14 [2] | | | | | | |
| | | V _{CC} = 1.2 V | - | 145 | - | - | - | ns |
| | | V _{CC} = 2.0 V | - | 51 | 93 | - | 110 | ns |
| | | V _{CC} = 2.7 V | - | 38 | 69 | - | 82 | ns |
| | | V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF | - | 25 | - | - | - | ns |
| | | V _{CC} = 3.0 V to 3.6 V | - | 30 | 56 | - | 66 | ns |
| | | V _{CC} = 4.5 V | - | 29 | 48 | - | 56 | ns |
| | | V _{CC} = 6.0 V | - | 21 | 37 | - | 44 | ns |
| | | Sn to Yn; see Fig. 14 [2] | | | | | | |
| | | V _{CC} = 1.2 V | - | 115 | - | - | - | ns |
| | | V _{CC} = 2.0 V | - | 41 | 73 | - | 90 | ns |
| | | V _{CC} = 2.7 V | - | 31 | 54 | - | 67 | ns |
| | | V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF | - | 20 | - | - | - | ns |
| | | V _{CC} = 3.0 V to 3.6 V | - | 24 | 44 | - | 54 | ns |
| | | V _{CC} = 4.5 V | - | 22 | 37 | - | 46 | ns |
| | | V _{CC} = 6.0 V | - | 17 | 29 | - | 36 | ns |
| C _{PD} | power dissipation capacitance | C _L = 50 pF; f _i = 1 MHz; V _I = GND to V _{CC} [3] | - | 25 | - | - | - | pF |

[1] All typical values are measured at nominal V_{CC} and at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

t_{en} is the same as t_{PZL} and t_{PZH}.

t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma((C_L + C_{SW}) \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz, f_o = output frequency in MHz

C_L = output load capacitance in pF

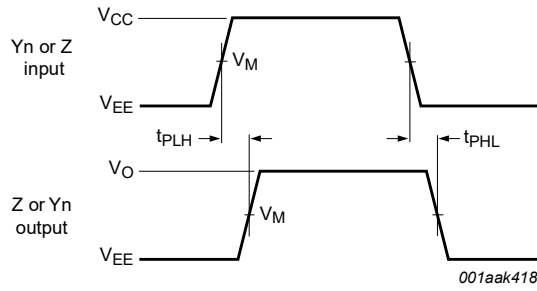
C_{SW} = maximum switch capacitance in pF;

V_{CC} = supply voltage in Volts

N = number of inputs switching

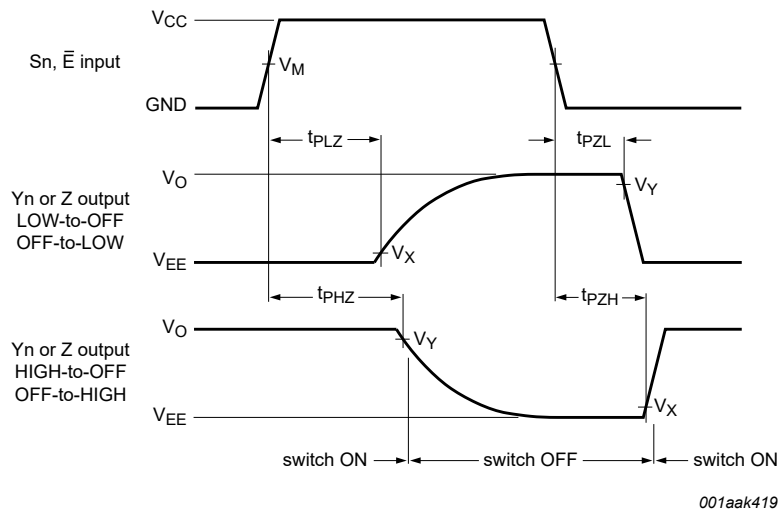
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

10.1. Waveforms and test circuit



Measurement points are given in Table 9.
 V_{EE} and V_O are typical voltage output levels that occur with the output load.

Fig. 13. Propagation delay input (Yn or Z) to output (Z or Yn)

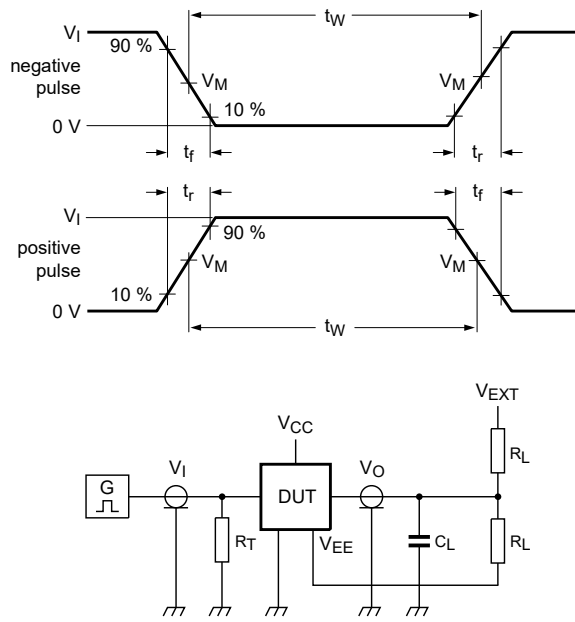


Measurement points are given in Table 9.
 V_{EE} and V_O are typical voltage output levels that occur with the output load.

Fig. 14. Enable and disable times

Table 9. Measurement points

| Supply voltage | Input | Output | | |
|----------------|-------------|-------------|----------------------|-------------------|
| V_{CC} | V_M | V_M | V_X | V_Y |
| < 2.7 V | $0.5V_{CC}$ | $0.5V_{CC}$ | $V_{EE} + 0.1V_{CC}$ | $V_O - 0.1V_{CC}$ |
| 2.7 V to 3.6 V | 1.5 V | 1.5 V | $V_{EE} + 0.3 V$ | $V_O - 0.3 V$ |
| > 3.6 V | $0.5V_{CC}$ | $0.5V_{CC}$ | $V_{EE} + 0.1V_{CC}$ | $V_O - 0.1V_{CC}$ |



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Test data is given in [Table 10](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 15. Test circuit for measuring switching times

Table 10. Test data

| Supply voltage | Input | | Load | | V_{EXT} | | |
|----------------|----------|-------------|--------------|--------------|--------------------|--------------------|--------------------|
| V_{CC} | V_I | t_r, t_f | C_L | R_L | t_{PHL}, t_{PLH} | t_{PZH}, t_{PHZ} | t_{PZL}, t_{PLZ} |
| < 2.7 V | V_{CC} | ≤ 6 ns | 50 pF | 1 k Ω | open | V_{EE} | $2V_{CC}$ |
| 2.7 V to 3.6 V | 2.7 V | ≤ 6 ns | 15 pF, 50 pF | 1 k Ω | open | V_{EE} | $2V_{CC}$ |
| > 3.6 V | V_{CC} | ≤ 6 ns | 50 pF | 1 k Ω | open | V_{EE} | $2V_{CC}$ |

10.2. Additional dynamic parameters

Table 11. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $V_I = \text{GND}$ or V_{CC} (unless otherwise specified); $t_r = t_f \leq 6.0 \text{ ns}$; $T_{amb} = 25 \text{ }^\circ\text{C}$.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------|---------------------------|---|-----|------|-----|------|
| THD | total harmonic distortion | $f_i = 1 \text{ kHz}$; $C_L = 50 \text{ pF}$; $R_L = 10 \text{ k}\Omega$; see Fig. 20 | | | | |
| | | $V_{CC} = 3.0 \text{ V}$; $V_I = 2.75 \text{ V (p-p)}$ | - | 0.8 | - | % |
| | | $V_{CC} = 6.0 \text{ V}$; $V_I = 5.5 \text{ V (p-p)}$ | - | 0.4 | - | % |
| | | $f_i = 10 \text{ kHz}$; $C_L = 50 \text{ pF}$; $R_L = 10 \text{ k}\Omega$; see Fig. 20 | | | | |
| | | $V_{CC} = 3.0 \text{ V}$; $V_I = 2.75 \text{ V (p-p)}$ | - | 2.4 | - | % |
| | | $V_{CC} = 6.0 \text{ V}$; $V_I = 5.5 \text{ V (p-p)}$ | - | 1.2 | - | % |
| $f_{(-3\text{dB})}$ | -3 dB frequency response | $C_L = 50 \text{ pF}$; $R_L = 50 \text{ }\Omega$; see Fig. 16 [1] | | | | |
| | | $V_{CC} = 3.0 \text{ V}$ | - | 180 | - | MHz |
| | | $V_{CC} = 6.0 \text{ V}$ | - | 200 | - | MHz |
| α_{iso} | isolation (OFF-state) | $f_i = 1 \text{ MHz}$; $C_L = 50 \text{ pF}$; $R_L = 600 \text{ }\Omega$; see Fig. 18 [2] | | | | |
| | | $V_{CC} = 3.0 \text{ V}$ | - | -50 | - | dB |
| | | $V_{CC} = 6.0 \text{ V}$ | - | -50 | - | dB |
| V_{ct} | crosstalk voltage | between digital inputs and switch; $f_i = 1 \text{ MHz}$; $C_L = 50 \text{ pF}$; $R_L = 600 \text{ }\Omega$; see Fig. 21 [2] | | | | |
| | | $V_{CC} = 3.0 \text{ V}$ | - | 0.11 | - | V |
| | | $V_{CC} = 6.0 \text{ V}$ | - | 0.12 | - | V |
| Xtalk | crosstalk | between switches; $f_i = 1 \text{ MHz}$; $C_L = 50 \text{ pF}$; $R_L = 600 \text{ }\Omega$; see Fig. 22 | | | | |
| | | $V_{CC} = 3.0 \text{ V}$ | - | -60 | - | dB |
| | | $V_{CC} = 6.0 \text{ V}$ | - | -60 | - | dB |

[1] Adjust f_i voltage to obtain 0 dBm level at output for 1 MHz (0 dBm = 1 mW into 50 Ω).

[2] Adjust f_i voltage to obtain 0 dBm level at output for 1 MHz (0 dBm = 1 mW into 600 Ω).

10.3. Test circuits

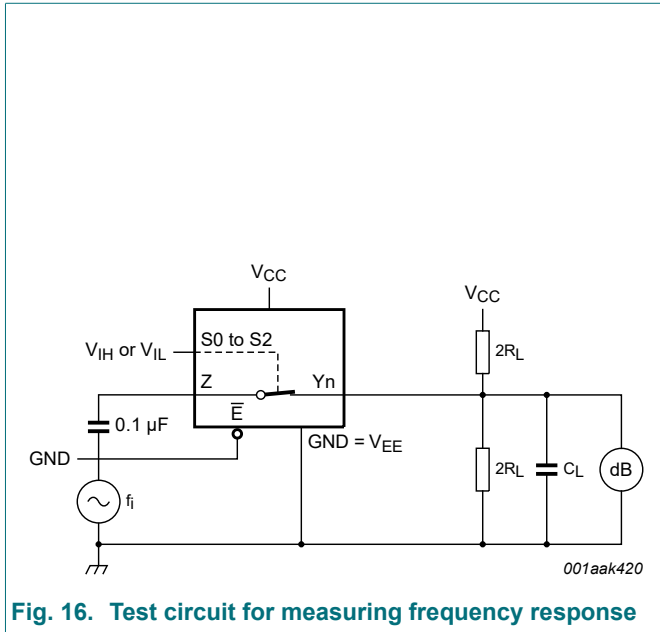


Fig. 16. Test circuit for measuring frequency response

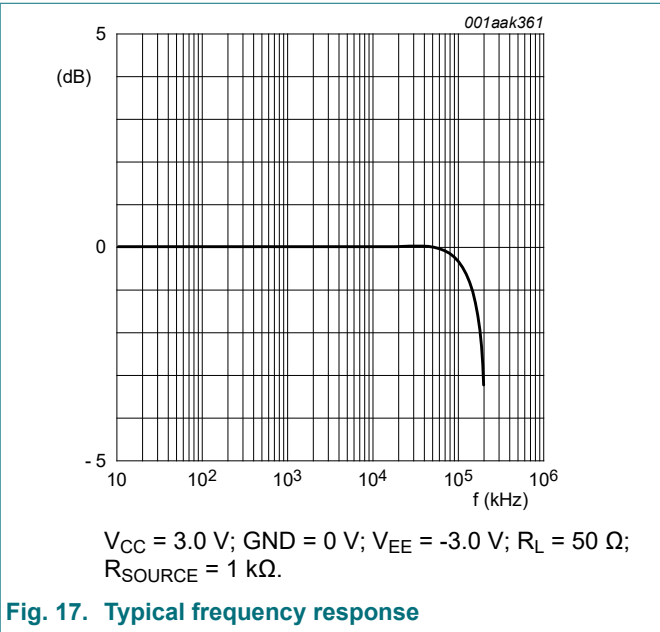


Fig. 17. Typical frequency response

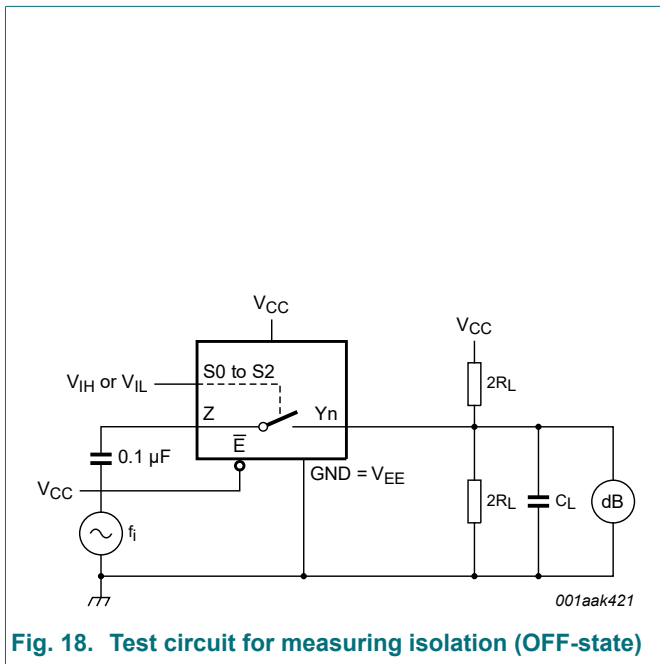


Fig. 18. Test circuit for measuring isolation (OFF-state)

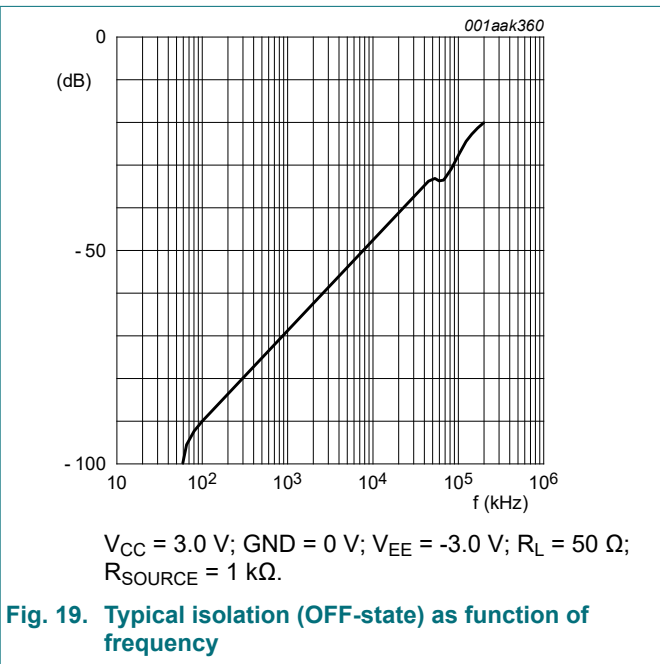


Fig. 19. Typical isolation (OFF-state) as function of frequency

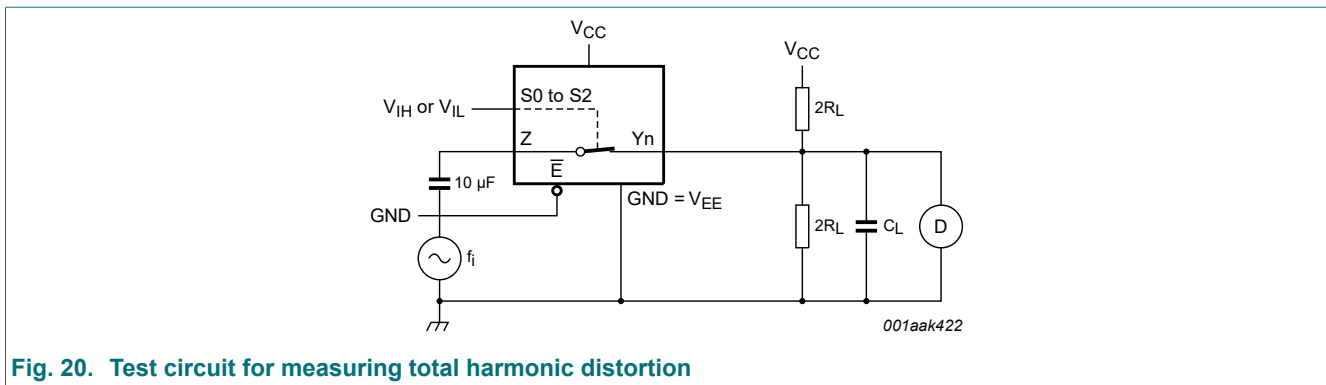
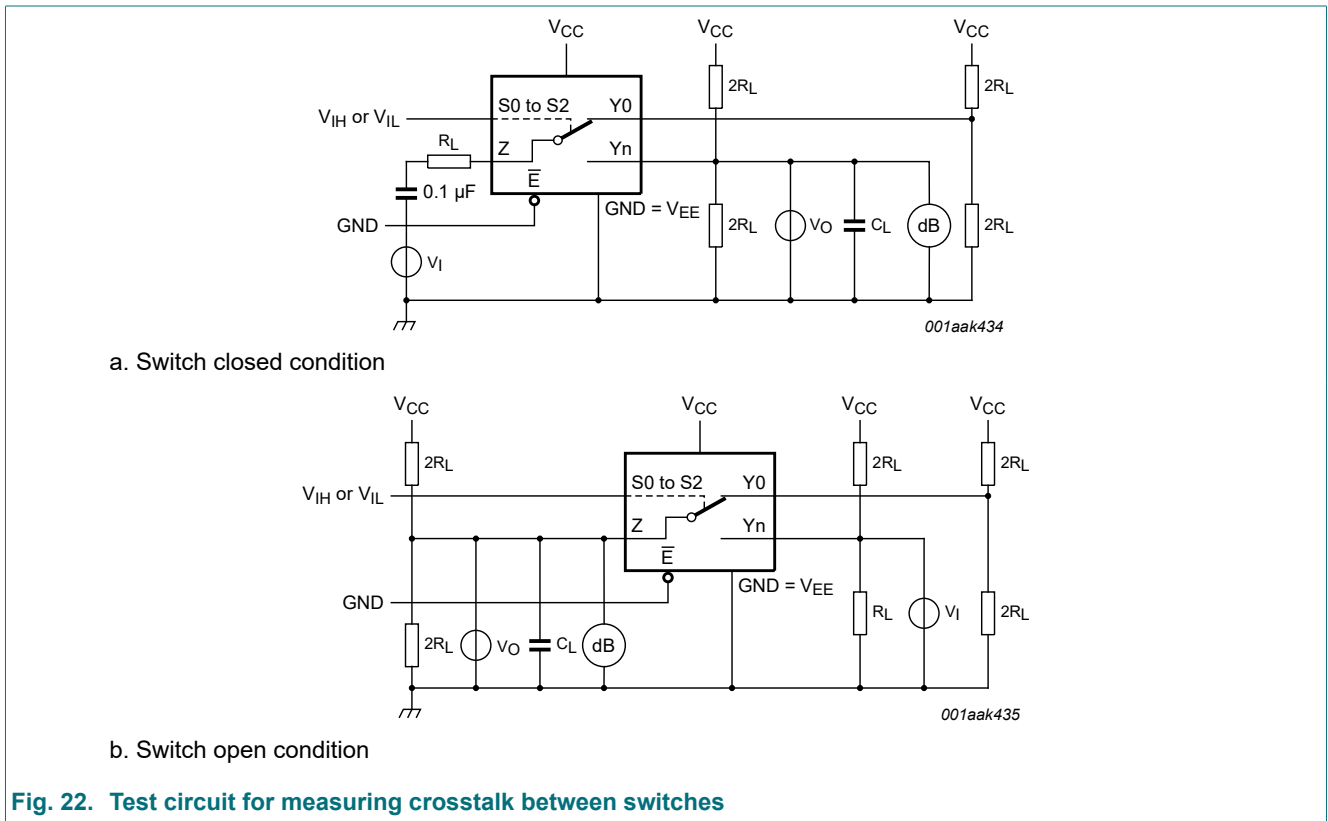
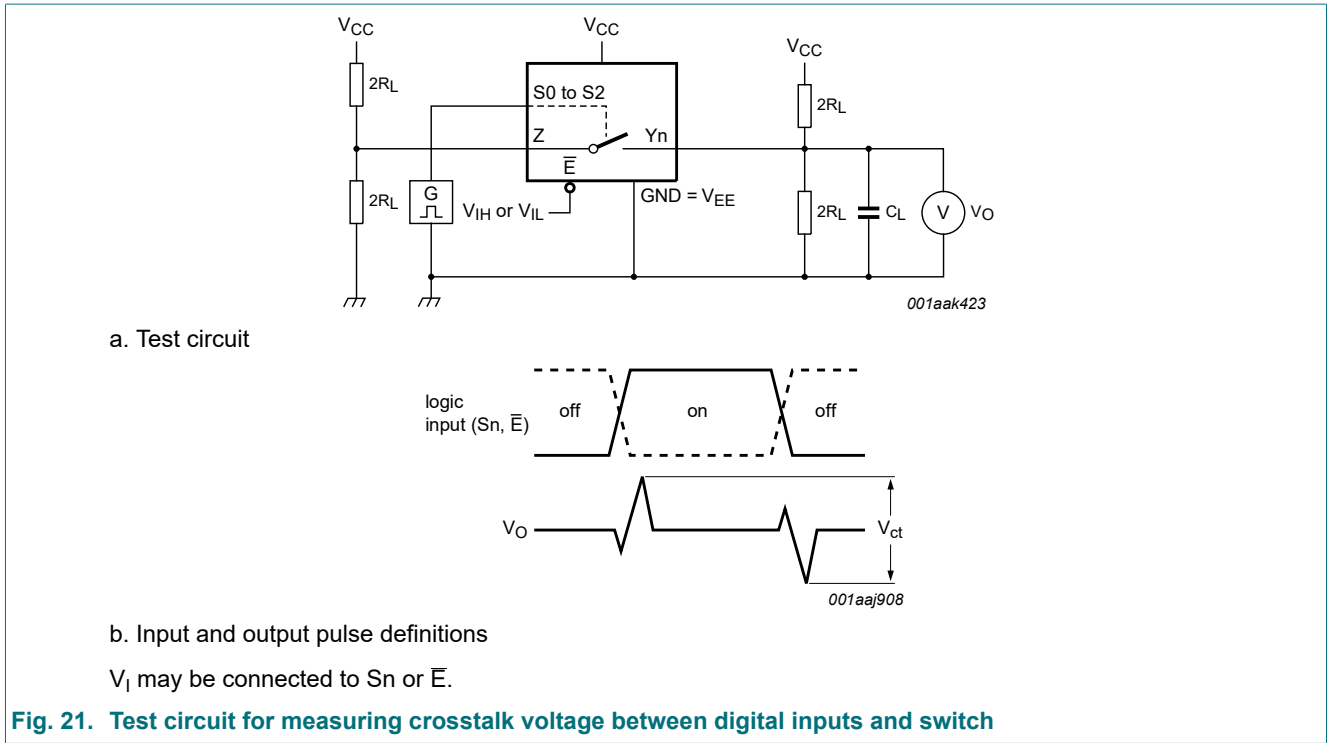


Fig. 20. Test circuit for measuring total harmonic distortion



11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

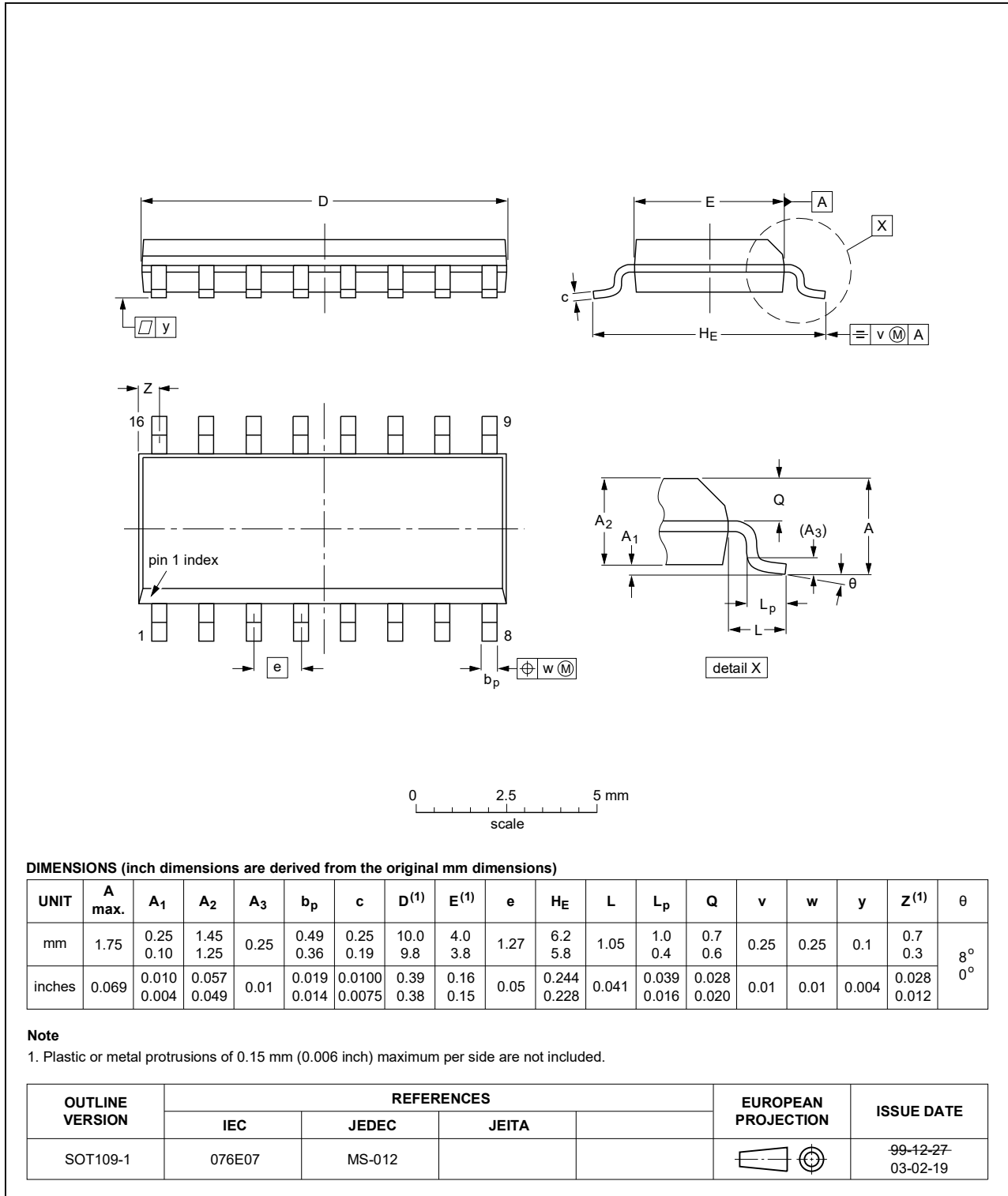


Fig. 23. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

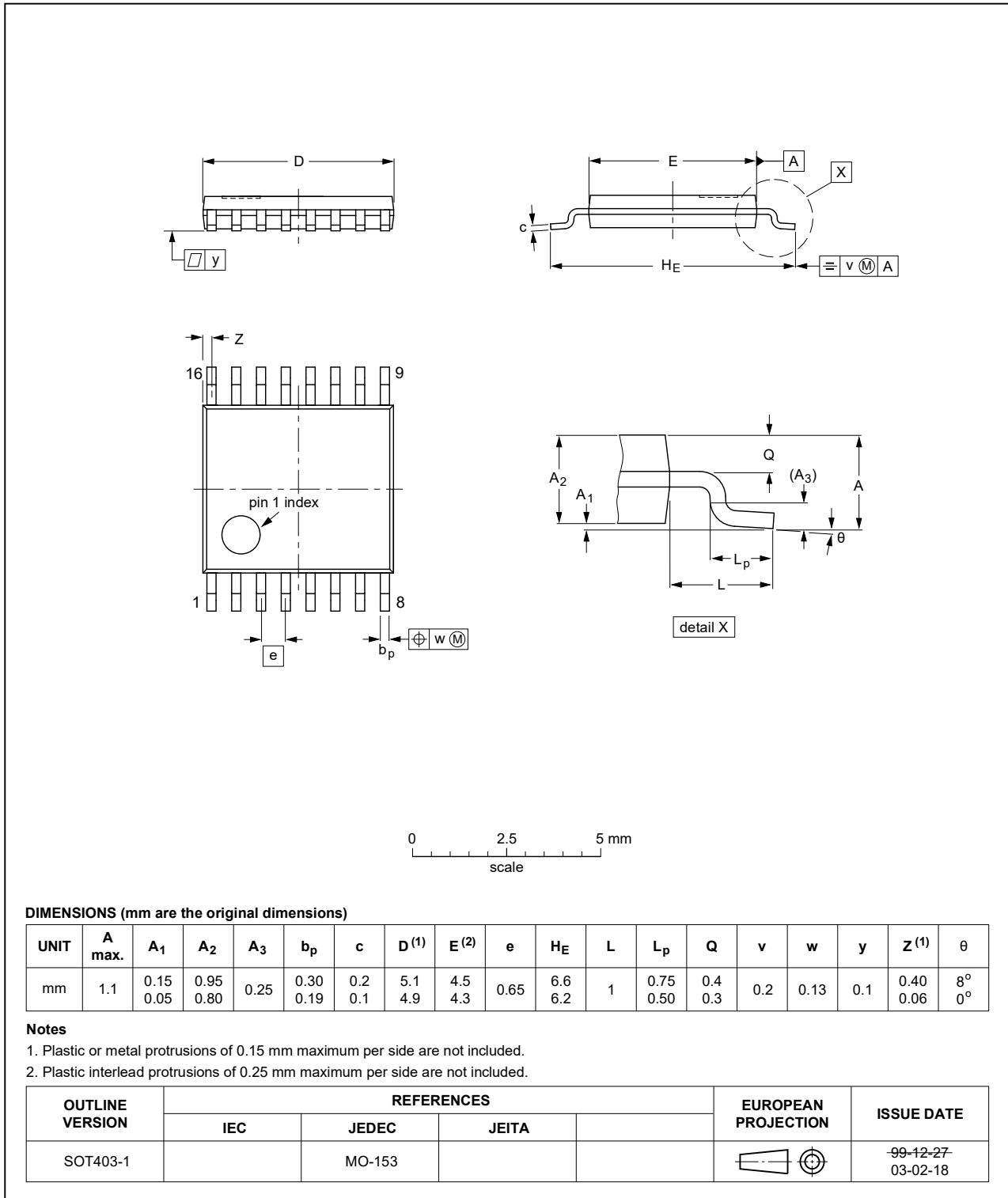


Fig. 24. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

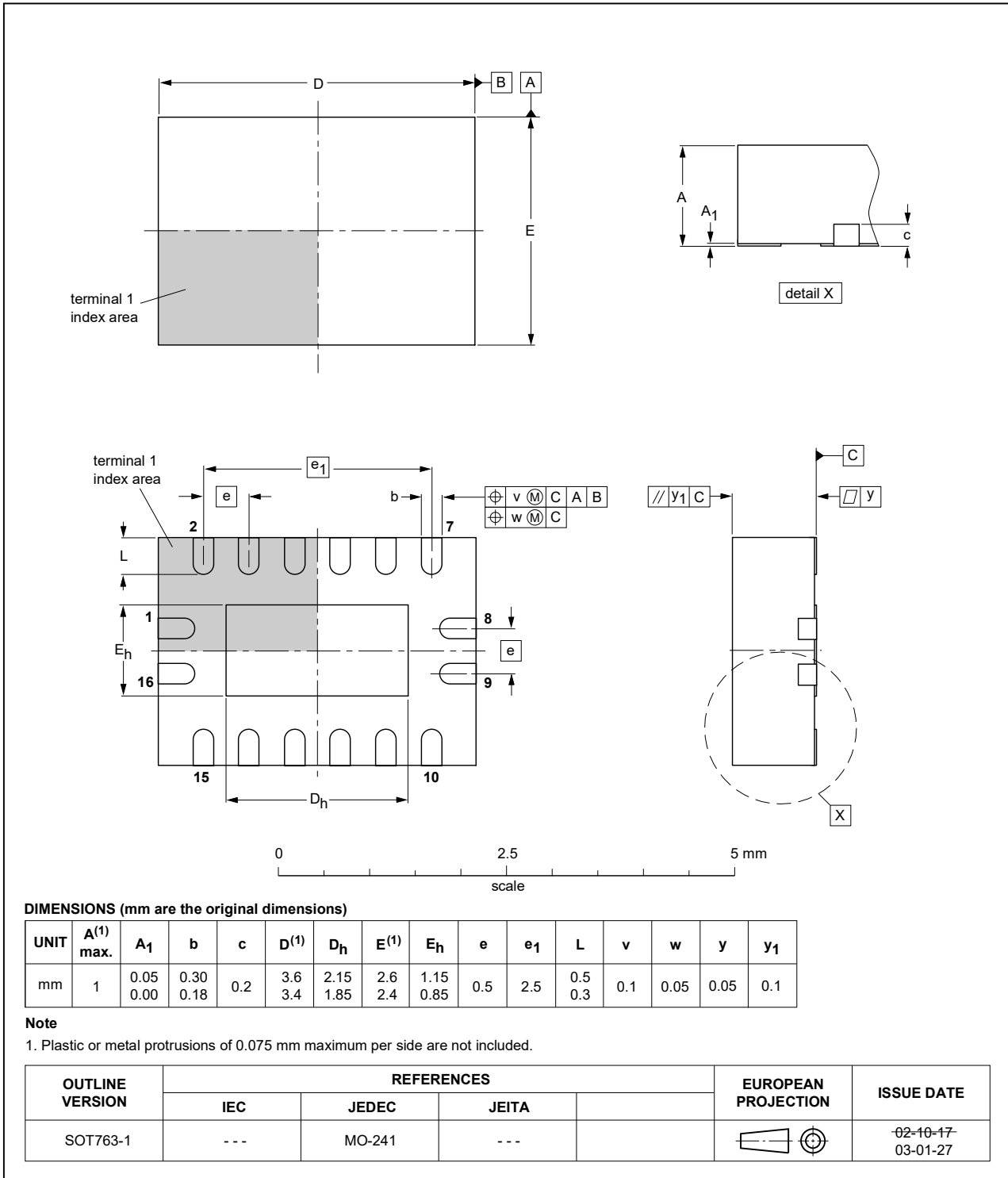


Fig. 25. Package outline SOT763-1 (DHVQFN16)

12. Abbreviations

Table 12. Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

13. Revision history

Table 13. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|--|-----------------------|---------------|--------------|
| 74LV4051 v.8 | 20210716 | Product data sheet | - | 74LV4051 v.7 |
| Modifications: | <ul style="list-style-type: none"> Type number 74LV4051DB (SOT338-1/SSOP16) removed. Section 7: Derating values for P_{tot} total power dissipation updated. | | | |
| 74LV4051 v.7 | 20181009 | Product data sheet | - | 74LV4051 v.6 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. | | | |
| 74LV4051 v.6 | 20160317 | Product data sheet | - | 74LV4051 v.5 |
| Modifications: | <ul style="list-style-type: none"> Type number 74LV4051N (SOT38-4) removed. | | | |
| 74LV4051 v.5 | 20140917 | Product data sheet | - | 74LV4051 v.4 |
| Modifications: | <ul style="list-style-type: none"> Fig. 7: Figure note added for DHVQFN16 package | | | |
| 74LV4051 v.4 | 20090810 | Product data sheet | - | 74LV4051 v.3 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Added type number 74LV4051BQ (DHVQFN16 package) | | | |
| 74LV4051 v.3 | 19960623 | Product specification | - | 74LV4051 v.2 |
| 74LV4051 v.2 | 19970715 | Product specification | - | 74LV4051 v.1 |

14. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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Contents

| | |
|--|-----------|
| 1. General description | 1 |
| 2. Features and benefits | 1 |
| 3. Ordering information | 1 |
| 4. Functional diagram | 2 |
| 5. Pinning information | 3 |
| 5.1. Pinning..... | 3 |
| 5.2. Pin description..... | 4 |
| 6. Functional description | 4 |
| 7. Limiting values | 4 |
| 8. Recommended operating conditions | 5 |
| 9. Static characteristics | 5 |
| 9.1. Test circuits..... | 6 |
| 9.2. ON resistance..... | 7 |
| 9.3. On resistance test circuit and graph..... | 8 |
| 10. Dynamic characteristics | 8 |
| 10.1. Waveforms and test circuit..... | 10 |
| 10.2. Additional dynamic parameters..... | 12 |
| 10.3. Test circuits..... | 13 |
| 11. Package outline | 15 |
| 12. Abbreviations | 18 |
| 13. Revision history | 18 |
| 14. Legal information | 19 |

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